AMENDMENTS TO THE CLAIMS

Claim 1. (Currently amended)

A charge sensing device comprising charge reference means and sense amplifier system, for sensing the charge of a passive addressable charge storing device, the ~~system~~ device comprising a pair of a first and second charge references connected in parallel and similar to the charge storing device, said first charge references having the opposite polarization of the second charge reference, said first and second charge references arranged to have a common input node with ~~and~~ the charge storing device ~~having a common input node~~; first and second pseudo differential reference sense amplifiers both being connected with output nodes of the respective charge reference, said first and second pseudo differential amplifiers being adapted for generating output reference signals to a common reference node; and a pseudo differential sense amplifier having a first input connected with the common reference node for receiving a common reference input signal and a second input ~~for receiving~~ arranged to receive an output signal from the charge storing device; whereby the pseudo differential sense amplifier is enabled to ~~perform a threshold comparison and generating an output sense signal indicative of a polarization state of the charge storing device~~ output a differential positive or negative signal which is converted to a digital logic level indicative of the polarization state of the charge-storing device depending on the sign of the differential sense signal.

Claim 2. (Previously Presented)

A charge sensing device according to claim 1, wherein both the pseudo differential reference sense amplifiers and the pseudo differential sense amplifier being identical pseudo differential sense amplifier circuits.

Claim 3. (Previously Presented)

A charge sensing device according to claim 2, wherein each pseudo differential sense amplifier circuit comprises input differential pair transistors connected with a pair of cascaded transistors, and current source biasing pair transistors cascaded with a pair of transistors, said cascading in each case increasing sense amplifier open loop gain.

Claim 4. (Previously Presented)

A charge sensing device according to claim 3, wherein input transistors being p channel transistors and the current source transistors n channel transistors, or vice versa.

Claim 5. (Previously Presented)

A charge sensing device according to claim 2, wherein each pseudo differential sense amplifier circuit comprises a semi balanced dual input with a balanced dual output.

Claim 6. (Previously Presented)

A charge sensing device according to claim 2, wherein that each pseudo differential sense amplifier circuit comprises a switched capacitor common feed back loop to control output common mode voltage.

Claim 7. (Previously Presented)

A charge sensing device according to claim 2, wherein each pseudo differential sense amplifier circuit comprises means for integral switched capacitor common mode self bias generation.

Claim 8. (Previously Presented)

A charge sensing device according to claim 2, wherein each pseudo differential sense amplifier circuit comprises an integral positive feed back latch.

Claim 9. (Previously Presented)

A charge sensing device according to claim 2, wherein each pseudo differential sense amplifier circuit comprises means for auto zero offset cancellation.

Claim 10. (Currently amended)

A charge sensing device for sensing the charges of a plurality of passive addressable charge storing device, comprising at least two pairs of a first and a second charge references arranged to be similar to the charge storing device, said first charge reference having the opposite

polarization of the second charge reference; each of said at least two pairs of charge references having a common input node and a pair of common output nodes respectively connected with said first and said second charge references in each of said at least two pairs thereof, each common input node of said at least two pairs of charge references moreover arranged to be ~~being~~ connected with at least two charge storing devices; first and second pseudo differential reference sense amplifiers being respectively connected with the first common output node and the second common output node of the charge reference, said first and second pseudo differential reference sense amplifiers being adapted for generating output reference signals to a common reference node; and at least two pseudo differential sense amplifiers, each having a first input connected with said common reference node for receiving a common reference input signal and a second input respectively arranged to be ~~being~~ connected with a common output node of respective one of said at least two charge storing devices for receiving respective output signals therefrom, said at least two charge storing devices forming the elements of an orthogonal row and column array thereof and with each of the charge storing devices of a row being connected to one of said at least two common input nodes and each of the charge storing devices of a column being connected to a common output node; whereby each pseudo differential sense amplifier is enabled to ~~perform~~ output ~~a threshold comparison and generating an output sense signal indicative of a polarization state of a selected charge storing device connected therewith~~ a differential positive or negative sense signal which is converted to a digital logic level indicative of a polarization state of the charge-storing devices depending on the sign of the differential sense signal.

Claim 11. (Previously Presented)

A charge sensing device according to claim 10, wherein the common input nodes forming a portion of the word line electrodes of a matrix addressable array of charge storing memory cells, the common output nodes of the charge reference device forming a pair of reference bit line electrodes the common output nodes of the charge storing device forming bit line electrodes of said matrix addressable array; each of the reference bit line electrodes being assigned to the first and second pseudo differential reference sense amplifiers respectively; and each of the other bit line electrodes being assigned to one of the pseudo differential sense amplifiers , whereby in a readout cycle a polarization state of respective selected charge storing memory cells can be detected either sequentially or in parallel and compared with a reference value.

Claim 12. (Previously Presented)

A charge sensing device according to claim 11, wherein the charge sensing device being provided as a subblock in a block of more than one charge sensing device of this kind, such that the sense amplifiers of a subblock are assigned to a corresponding number of bit line electrodes in the matrix addressable array; and the pair of reference bit lines of respective subblocks being distributed among the bit lines of array.

Claim 13. (Previously Presented)

A charge sensing device according to claim 11, wherein that the sense amplifier system comprises a multiplexer connected with the bit line electrodes of the matrix addressable array; a number k of consecutive bit lines in the array defining a segment of all word line electrodes

therein, said number k of segment defining bit lines corresponding to the number of pseudo differential sense amplifiers in the charge sensing device; and a pair of reference bit line electrodes being provided adjacent to the bit line electrodes in each word line segment and connecting pairs of reference charge storing devices in each word line segment; whereby the charge storing memory cells on a single word line electrode of a word line segment may be read in parallel, and all word line segments similarly in turn by applying an appropriate addressing protocol and multiplexing the bit line electrodes of a selected word line segment to establish their parallel connection to respective pseudo differential sense amplifiers of the charge sensing device as provided.

Claim 14. (Previously Presented)

A non-volatile passive matrix addressable memory device comprising an electrically polarizable dielectric memory material exhibiting hysteresis, particularly a ferroelectric or electret material, wherein said memory material is provided in a layer contacting a first set and second set of respective parallel addressing electrodes, wherein the electrodes of the first set constitute word lines of the memory device and are provided in substantially orthogonal relationship to the electrodes of the second set, the latter constituting bit lines of the memory device, wherein memory cells with a capacitor like structure are defined in the memory material at the crossings between word lines and bit lines, wherein each memory cell can be selectively addressed for a write/read operation via a word line and bit line, wherein a write operation to a memory cell takes place by establishing a desired polarization state in the cell by means of a voltage being applied to the cell via the respective word line and bit line defining the cell,

wherein said applied voltage either establishes a determined polarization state in the memory cell or is able to switch between the polarization states thereof, wherein a read operation takes place by applying a voltage to the memory cell and detecting at least one electrical parameter of an output current on the bit lines, wherein at least one charge sensing device is provided for sensing said polarization states of said memory cells during a read operation, and wherein said at least one charge sensing device is a pseudo-differential sense amplifier system comprising at least one system subblock, and that said at least one system subblock comprises at least one pseudo differential sense amplifier circuit for sensing a polarization state of at least one memory cell during said read operation and two reference sense amplifier circuits for sensing polarization states of two reference memory cells during said read operation, said reference ferroelectric memory cells having opposite polarization states said pseudo differential reference sense amplifier circuit being connected with said at least one pseudo-differential sense amplifier circuit via a common node.

Claim 15. (Previously Presented)

A memory device according to claim 14, wherein said at least one system subblock comprises a plurality of said pseudo-differential sense amplifier circuits for sensing respective polarization states of a corresponding plurality of memory cells during said read operation.

Claim 16. (Canceled)

Claim 17. (Previously Presented)

A memory device according to claim 16, wherein the first and the second reference sense amplifier circuits are adapted for generating an average of a first and a second reference memory cell output signal to said common node, and that said at least one sense amplifier circuit connected therewith is adapted for comparing the output signal at said common node with the output signal from a memory cell.

Claim 18. (Previously Presented)

A memory device according to claim 14, wherein said at least one sense amplifier circuit and said at least one reference sense amplifier circuit are realized with identical amplifier circuitry.

Claim 19. (Previously Presented)

A memory device according to claim 18, wherein said identical amplifier circuitry comprises a reference side and an array side, said reference side mirroring the circuit structure of said array side.

Claim 20. (Previously Presented)

A memory device according to claim 14, wherein said pseudo differential sense amplifier system comprises a plurality of system subblocks.

Claim 21. (Previously Presented)

A memory device according to claim 20, wherein each subblock comprises a plurality of said sense amplifier circuits for sensing the polarization state of a corresponding number of memory cells.